Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-15 (Canceled)

Claim 16 (Currently amended): A semiconductor wafer comprising:

a plurality of dies each comprising functional circuitry;

electrically conductive structures configured to contactlessly receive test signals from a test board in physical proximity to said wafer for testing said functional circuitry of said dies; and

an electrically conductive shielding plane disposed between at least part of ones of said conductive structures and at least part of said functional circuitry of ~~at least one of~~ said dies, said shielding plane shielding said dies from electrical interference.

Claim 17 (Original): The semiconductor wafer of claim 16, wherein each die comprises a set of said conductive structures.

Claim 18 (Currently amended): The semiconductor wafer of claim [[16]] 17, wherein each of said conductive structures in a set of said conductive structures are electrically connected to a plurality of said dies.

Claim 19 (Canceled)

Claim 20 (Original): The semiconductor wafer of claim 16 further comprising a transmitter configured to transmit test signals on at least one of said conductive structures.

Claim 21 (Original): The semiconductor wafer of claim 20, wherein each of said dies comprises such a transmitter.

Claim 22 (Original): The semiconductor wafer of claim 16 further comprising a receiver configured to receive a test signal induced on at least one of said conductive structures.

Claim 23 (Original): The semiconductor wafer of claim 22, wherein each of said dies comprises such a receiver.

Claim 24 (Original): The semiconductor wafer of claim 16 further comprising a transceiver configured to transmit test signals on at least one of said conductive structures and to receive a test signal induced on at least one of said conductive structures.

Claim 25 (Original): The semiconductor wafer of claim 24, wherein each of said dies comprises such a transceiver.

Claim 26 (Original): The semiconductor wafer of claim 16 further comprising built in self test circuitry.

Claim 27 (Currently amended): A semiconductor wafer comprising:

a plurality of dies each comprising functional circuitry;

means for receiving [[a]] test signals from ones of a plurality of tester channels on a test board in physical proximity to said wafer without physically contacting said tester channels; and

an electrically conductive shielding plane disposed between at least part of said means for receiving [[a]] test signals and at least part of said functional circuitry ~~of at least one~~ of said dies, said shielding plane shielding said dies from electrical interference.

Claim 28 (Currently amended): The semiconductor wafer of claim 27 further comprising means for sending [[a]] test signals to [[a]] ones of said tester channels without physically contacting said tester channels.

Claim 29 (Canceled)

Claim 30 (Currently amended): The semiconductor wafer of claim 27 further comprising means for controlling communications with ~~a plurality of~~ said tester channels.

Claims 31-35 (Canceled)

Claim 36 (Currently amended): The semiconductor wafer of claim 27, wherein:

each die further comprises communications control circuitry; and

~~ones of~~ said means for receiving [[a]] test signals [[are]] is electrically connected to said communications control circuitry through openings in said plane.

Claim 37 (Currently amended): The semiconductor wafer of claim 36, wherein ~~at least one of~~ said means for receiving [[a]] test signals is electrically connected ~~to said communications control circuitry and~~ to said plane.

Claim 38 (Previously presented): The semiconductor wafer of claim 37, wherein said plane is a ground plane.

Claim 39 (Previously presented): The semiconductor wafer of claim 16 further comprising:

a plurality of electrically conductive planes disposed between said conductive structures and said functional circuitry; and

insulating material disposed between said planes.

Claim 40 (Currently amended): The semiconductor wafer of claim 39, wherein one of said planes is configured as a power distribution plane, and another of said planes is configured as a ground plane, wherein one of said power distribution plane or said ground plane comprises said shielding plane.

Claim 41 (Previously presented): The semiconductor wafer of claim 16, wherein:

each die further comprises communications control circuitry; and

ones of said conductive structures are electrically connected to said communications control circuitry through openings in said plane.

Claim 42 (Previously presented): The semiconductor wafer of claim 41, wherein at least one of said conductive structures is electrically connected at one end to said communications control circuitry and is electrically connected at another end to said plane.

Claim 43 (Previously presented): The semiconductor wafer of claim 42, wherein said plane is a ground plane.

Claim 44 (Previously presented): The semiconductor wafer of claim 27 further comprising:

a plurality of electrically conductive planes disposed between said conductive structures and said functional circuitry; and

insulating material disposed between said planes.

Claim 45 (Currently amended): The semiconductor wafer of claim 44, wherein one of said planes is configured as a power distribution plane, and another of said planes is configured as a ground plane, wherein one of said power distribution plane or said ground plane comprises said shielding plane.

Claim 46 (Canceled)

Claim 47 (Currently amended): The semiconductor wafer of 16, wherein said electrically conductive shielding plane is sized to substantially cover ~~at least one of~~ said dies.

Claim 48 (Canceled)

Claim 49 (Currently amended): The semiconductor wafer of 27, wherein said electrically conductive shielding plane is sized to substantially cover ~~at least one of~~ said dies.

Claim 50 (Currently amended): The semiconductor wafer of 16, wherein said shielding plane comprises openings through which said conductive structures are electrically connected to said functional circuitry of ~~said at least one of~~ said dies.

Claim 51 (Previously presented): The semiconductor wafer of claim 47, wherein said shielding plane is a solid plate structure.

Claim 52 (Currently amended): The semiconductor wafer of 27, wherein said shielding plane comprises openings through which said means for receiving [[a]] test signals is electrically connected to said functional circuitry of said at least one of said dies.

Claim 53 (Previously presented): The semiconductor wafer of claim 49, wherein said shielding plane is a solid plate structure.

Claim 54 (New): The semiconductor wafer of claim 41, wherein said communications control circuitry is configured to control communication of said test signals through said conductive structures to said test board, said communication control circuitry further configured to control communication of said test signals into and output of said functional circuitry of said die.

Claim 55 (New): The semiconductor wafer of claim 36, wherein said communications control circuitry is configured to control communication of said test signals through said conductive structures to said tester channels on said test board, said communication control circuitry further configured to control communication of said test signals into and output of said functional circuitry of said die.